UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/992,880	11/05/2001	James D. Beasom	125.014US01	7668

7590 11/29/2002

Fogg, Slifer & Polglaze, P.A.
P.O. Box 581009
Minneapolis, MN 55458-1009

EXAMINER	
PHAM, HOAI V	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 11/29/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/992,880	JAMES D. BEASOM	
	Examiner	Art Unit	
	Hoai V Pham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 September 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,8-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *33-37* is/are allowed.

6)☒ Claim(s) *1-5,8-17,20 and 23-29* is/are rejected.

7)☐ Claim(s) *18,19,21,22 and 30-32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim 13 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The phrase "to access selected device regions formed in the substrate by the implanted ions" is not supported in the specification since claim 10 does not recited the access selected device regions formed in the substrate by the implanted ions.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-5, 8-17, 20, 23, 24, and 29 are rejected under 35 U.S.C. 102(b) as being anticipated by Chang et al. [U.S. Pat. 5,792,681] previously applied.

Chang et al. (figs. 1-10, cols. 3-5) discloses a method of forming a contact opening through a dielectric layer (14) overlaying an oxide layer (9) in an integrated circuit, the method comprising:

forming a layer of mask material (18) overlaying the dielectric layer (fig.9, col. 5, lines 11-15);

patterning the layer of mask material to expose a pre-selected portion of the dielectric layer (fig.9, col. 5, lines 11-15); and

forming anisotropic contact openings (in regions 3-4) that extend through the layer of dielectric (14) and the layer of oxide (9) using a dry etch with a single mask (fig.9, col. 5, lines 14-22).

With respect to claim 2, Chang et al. discloses removing the layer of mask material (see fig. 10).

With respect to claim 3, Chang et al. discloses that the mask material (18) is photo resist mask material (see col. 5, line 14).

With respect to claim 4, Chang et al. discloses that the pattering of the layer of mask material further comprises: removing a portion of the mask material adjacent a portion of the dielectric layer where the contact opening is to be formed (see fig. 9).

With respect to claim 5, Chang et al. discloses that the dry etch used is a reactive ion dry etch (see col. 5, lines 14-23).

With respect to claims 8 and 9, Chang et al. discloses that the dielectric constant of the dielectric layer is higher than the dielectric constant of the layer of oxide and wherein the dielectric (14) is silicon nitride (see col. 4, lines 42-43).

With respect to claim 10, Chang et al. (figs. 1-10, cols. 3-5) discloses a method of forming an integrated circuit, the method comprising:

forming an oxide layer (9) on a surface of a substrate (1), the substrate having a plurality of isolation islands, wherein at least one isolation island is used in forming a semiconductor device (fig. 2, col. 3, lines 64-65);

patterning the oxide layer to expose predetermined areas of the surface of the substrate (fig. 3, col. 4, lines 4-12);

depositing a nitride layer (14) overlaying the oxide layer and the exposed surface areas of the substrate, wherein the nitride layer is in contact with the oxide layer and all of the exposed surface areas created by the patterning the oxide layer (fig. 6, col. 4, lines 42-46); and

implanting ions through the nitride layer, wherein the nitride layer is an implant screen for the implanted ions (fig. 7, col. 4, lines 59-66);.

With respect to claim 11, Chang et al. discloses diffusing the ions to form device regions (16b) in selected isolation islands in the substrate (see fig. 8).

With respect to claim 12, Chang et al. discloses using the nitride layer in at least one of the isolation islands as a capacitor dielectric in forming a capacitor (5) (see figs. 8-10).

With respect to claim 13, as best understood, Chang et al. discloses performing a dry etch to form anisotropic contact openings (in regions 3-4) that extend through the layer nitride (14) and the layer of oxide (9) (fig.9, col. 5, lines 14-22).

With respect to claim 14, Chang et al. discloses that the dry etch used is a reactive ion dry etch (see col. 5, lines 14-23).

With respect to claim 15, Chang et al. (figs. 1-10, cols. 3-5) discloses a method of forming an integrated circuit, the method comprising:

forming an oxide layer (9) on a surface of a substrate (1), the substrate having a plurality of isolation islands, wherein at least one isolation island is used in forming a semiconductor device (fig. 2, col. 3, lines 64-65);

patterning the oxide layer to expose predetermined areas of the surface of the substrate (fig. 3, col. 4, lines 4-12);

depositing a nitride layer (14) overlaying the oxide layer and the exposed surface areas of the substrate, wherein the dielectric layer has a higher dielectric constant than a dielectric constant of the oxide layer, further wherein the dielectric layer is in contact with the oxide layer and all of the exposed surface areas created by the patterning the oxide layer (fig. 6, col. 4, lines 42-46); and

implanting ions through the nitride layer (fig. 7, col. 4, lines 59-66);

diffusing the ions to form device regions (16b) in selected isolation islands in the substrate (figs. 7-8, col. 4, lines 59-66; col. 5, lines 1-10); and

using the dielectric layer (14) in at least one of the isolation islands as a capacitor dielectric in forming a capacitor (5) (see figs. 8-10).

With respect to claim16, Chang et al. discloses that the capacitor dielectric layer (14) is a layer of silicon nitride (see col. 4, lines 42-43).

With respect to claim17, Chang et al. discloses forming contact openings to the device regions (13b, 16b) (see fig. 9-10).

With respect to claim 20, Chang et al. discloses depositing a layer of metal (20a) overlaying the layer of nitride and the exposed device regions through the contact openings; and patterning the layer of metal contacts to form metal contact regions for each contact opening (see fig. 10, col. 5, lines 34-39).

With respect to claim 23, Chang et al. (figs. 1-10, cols. 3-5) discloses a method of forming an integrated circuit, the method comprising:

forming an oxide layer (9) on a surface of a substrate (1), the substrate having a plurality of isolation islands, wherein at least one isolation island is used in forming a semiconductor device (fig. 2, col. 3, lines 64-65);

patterning the oxide layer to expose predetermined areas of the surface of the substrate (fig. 3, col. 4, lines 4-12);

implanting and diffusing ions (13a) into the substrate to form device regions(13b) (see fig. 5-6, col. 4, 47-50);

forming a dielectric layer (14) overlaying the oxide layer and the exposed areas of the surface of the substrate, wherein the dielectric layer has a dielectric constant higher than a dielectric constant of the oxide layer, further wherein the dielectric layer is in contact with the oxide layer and all of the exposed surface areas created by the patterning the oxide layer (fig. 6, col. 4, lines 42-46); and

using the dielectric layer in at least one of the isolation islands as a capacitor dielectric in forming a capacitor (5) (see figs. 8-10).

With respect to claim 24. Chang et al. discloses that the dielectric layer is a nitride layer formed by low pressure chemical vapor deposition (see col. 4, lines 42-45).

With respect to claim 29. Chang et al. discloses forming contact openings to the device regions (13b, 16b) (see fig. 9-10).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 25 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. [U.S. Pat. 5,792,681] previously applied, in view of Schroeder [U.S. Pat. 4,296,429] newly cited.

With respect to claim 25, Chang et al. does not mention using open tube deposition as a dopant source to form the device regions. However, Schroeder shows using open tube deposition as a dopant source to form the device regions (14) into the groove (16) (col. 4, lines 3-8). Therefore, it would have been obvious to the skilled in the art to use the open tube deposition method in the device of Chang et al. in order to form the device regions with heavily doped junctions since such a method is well known as taught by Schroeder.

With respect to claim 27, Chang et al. discloses a non-selective etch is used to expose the surface of the substrate adjacent device region before the dielectric is formed (col. 4, 13-15).

With respect to claim 28, Chang et al. discloses that the non-selective etch uses a wet etchant containing hydrogen fluoride (col. 3, lines 42-44).

7. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. [U.S. Pat. 5,792,681] previously applied, and Schroeder [U.S. Pat. 4,296,429] newly cited, as applied to claim 25 above, and further in view of Choi [U.S. Pat. 5,780,330] newly cited.

Chang et al. does not disclose that the dopant source is phosphorus oxychloride. However, Choi shows that the dopant source is phosphorus oxychloride to form source/drain regions (6, 7) (col. 9, lines 64-68, col. 10, lines 1-2). Therefore, it would have been obvious to the skilled in the art to use phosphorus oxychloride in the device of Chang et al. to form source/drain regions (6, 7) since such a dopant is well known as taught by Choi.

Allowable Subject Matter

8. Claims 33-37 are allowed.

9. Claims 18, 19, 21, 22, and 30-32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matter: the prior art of record fails to disclose diffusing the dopants to form a bottom plate in the capacitor isolation island and an emitter and collector contact in the transistor isolation island.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoai V Pham whose telephone number is 703-308-6173. The examiner can normally be reached on 6:30A.M. - 6:00P.M..

12. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 703-308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

13. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

HP
Hoai Pham
November 26, 2002

SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800